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**V. REMARKS**

Claims 1, 2, 4, 5, 7, 8 and 18-20 are rejected under 35 U.S.C. 102(a) as anticipated by Nakazawa (U.S. Patent No. 6,228,665). The rejection is respectfully traversed.

Nakazawa discloses a semiconductor package that has a wiring substrate 11, a semiconductor element 12 face-down-bonded to the surface of the wiring substrate 11 and a mold layer 13 permanently joined to the surface of the wiring substrate 11 and covering the sidewall of the semiconductor element 12 with an inactive surface of the semiconductor element 12 exposed to the outside of the mold layer 13. Between the semiconductor element 12 and the wiring substrate 11, bumps 16 are provided for interconnection therebetween and an under-fill 19 surrounding the bumps 16. Solder balls 18 are provided on the lower surface of the wiring substrate 11.

Claim 7 is directed to a semiconductor device that includes a board, a semiconductor chip and a protective resin. Claim 7 recites that the board having a mounting surface and an opposite surface and the semiconductor chip is mounted on the mounting surface of the board with the semiconductor chip having an active surface and an inactive surface disposed opposite the active surface and with the semiconductor chip being joined to the board in a state where the active surface thereof is facing to the board and the inactive surface thereof is exposed. Claim 7 also recites that the protective resin is permanently joined to the mounting surface of the board covering a sidewall of the semiconductor chip with the inactive surface thereof exposed to the outside of the protective resin, having a surface formed so as to be flush with an inactive surface of the semiconductor chip and having a side surface formed so as to be flush with a side surface of the board along a plane perpendicular to the mounting surface of the board.

It is respectfully submitted that the rejection is improper because the applied art fails to teach each element of claim 7. Specifically, the applied art fails to teach a protective resin that has a surface formed so as to be flush with an inactive surface of the semiconductor chip and having a side surface formed so as to be flush with a side surface of the board along a plane perpendicular to the mounting surface of the board. Thus, it is respectfully submitted that claim 7 is allowable over the applied art.

Claims 1, 2 and 8 depend from claim 7 and include all of the features of claim 7. It is respectfully submitted that the dependent claims are allowable at least for the reasons claim 7 is allowable as well as for the features they recite.

Claims 4, 5 and 18-20 are canceled and therefore the rejection as applied thereto is now moot.

Withdrawal of the rejection is respectfully requested.

Claims 6 and 9 are rejected under 35 U.S.C. 103(a) as unpatentable over Nakazawa as applied to Claims 1, 2, 4, 5, 7, 8 and 18-20 and further in view of Hikita et al. (U.S. Patent No. 6,376,915). The rejection is respectfully traversed.

Claims 6 and 9 are canceled and therefore the rejection as applied thereto is now moot.

Withdrawal of the rejection is respectfully requested.

Newly-added claims 21-23 also include features not shown in the applied art.

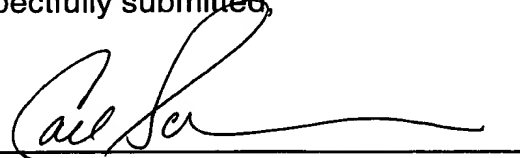
In view of the foregoing, reconsideration of the application and allowance of the pending claims are respectfully requested. Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicants' representative at the telephone number listed below.

Should additional fees be necessary in connection with the filing of this paper or if a Petition for Extension of Time is required for timely acceptance of the same, the Commissioner is hereby authorized to charge Deposit Account No. 18-0013 for any such fees and Applicant(s) hereby petition for such extension of time.

Respectfully submitted,

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